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(72) Inventors:
• Elliot, William D.
Sunnyvale, California 94086 (US)
• Neugebauer, Charles
Palo Alto, California 94301 (US)

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(74) Representative: Palmer, Roger et al
PAGE, WHITE & FARRER
54 Doughty Street
London WC1N 2LS (GB)

(71) Applicant: **STMicroelectronics, Inc.**
Carrollton Texas 75006-5039 (US)

(54) **Digital phase lock loop**

(57) A system includes an all digital circuit implementation and standard cell construction of PLL (108) with a digital frequency synthesizer and a digital phase detector (224). The synthesizer includes a digital DLL (202) including a plurality of delay chains, each including at least one digitally programmable delay element to achieve a phase lock with an input reference signal. The synthesizer also comprises a non-glitching MUX (206) electrically coupled to the digital DLL (202) for selecting a tap output from one of the delay elements to select at least one pulse glitch-free from the selected output tap,

and a phase accumulator (208) electrically coupled to the MUX (206) for precisely dividing a timing period of the input reference signal and selecting a tap output from one delay element to select at least one pulse at a precise point in the timing period from the output tap. The phase detector (224), is electrically coupled to the synthesizer to compare an edge of the input reference signal to an edge of a synthesized signal to provide information representing a phase error between the edge of the input reference signal and the edge of the synthesized signal.

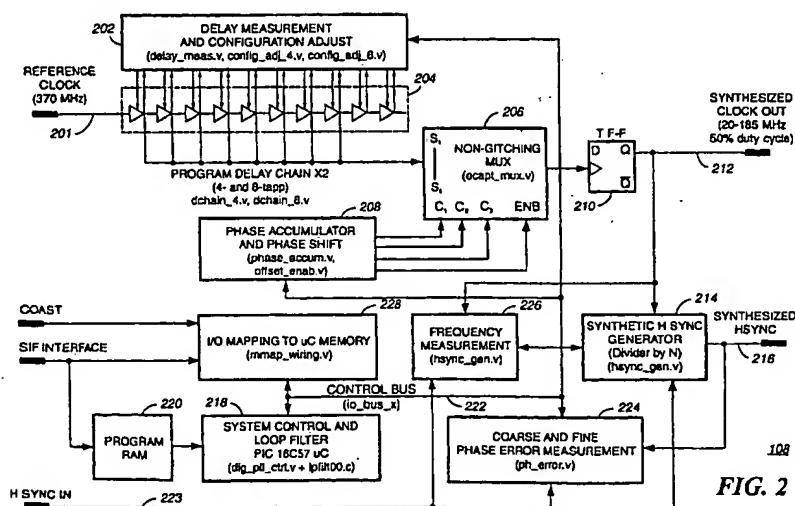


FIG. 2

European Patent
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EUROPEAN SEARCH REPORT

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			H03L G09G
The present search report has been drawn up for all claims			
Place of search MUNICH		Date of completion of the search 10 June 2003	Examiner Kahn, K-D
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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ANNEX TO THE EUROPEAN SEARCH REPORT
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